Very high growth rate epitaxy processes with chlorine addition.

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Abstract. The growth rate of 4H-SiC epi layers has been increased by a factor 19 (up to 112 μm/h) with respect to the standard process with the introduction of HCl in the deposition chamber. The epitaxial layers grown with the addition of HCl have been characterized by electrical, optical and structural characterization methods. An optimized process without the addition of HCl is reported for comparison. The Schottky diodes, manufactured on the epitaxial layer grown with the addition of HCl at 1600 °C, have electrical characteristics comparable with the standard epitaxial process with the advantage of an epitaxial growth rate three times higher.

Introduction

Recently several works on high voltage SiC devices with breakdown voltages of about *10 kV* have been published. This voltage capability can be obtained using wide band gap materials like SiC and consequently there is no competition with silicon power devices. These new devices include: power DMOSFET[1], implanted VJFET[2], PiN diodes[3] and Schottky diodes[4]. To obtain a breakdown voltage between 10 and 11 kV an epitaxial layer thickness in the region of *80-100 μm* is needed. Obviously to obtain this layer thickness with a standard epitaxial growth rate of *6-8 μm/h* a process time of more than ten hours with a consequently high processing cost is required.

The homoepitaxial growth of *α-SiC* has been achieved by chemical vapor deposition (CVD) methods. The epitaxial growth rate increases proportionally to the SiH_4 flow but for high SiH_4 flows *Si* droplets are formed in the gas phase and are then deposited on the wafer.

A new epitaxial process that overcomes this limitation has been recently developed[5] and it represents a breakthrough in the epitaxy process. The growth rate has been increased with respect to the standard process by increasing the silane flow combined with the introduction of *HCl* in the deposition chamber. Now a much higher growth rate (112 μm/h) with a good surface morphology can be obtained. In this paper, 4H-SiC epitaxial layers have been grown using both the process with HCl addition and trichlorosilane (TCS) as silicon precursor source together with ethylene as carbon precursor source. TCS is the typical precursor used in silicon epitaxy for its safety and stability in industrial processes and should avoid the homogeneous nucleation of silicon droplets in the gas phase. In fact, the simple replacement of SiH_4 with $SiHCl_3$ *(TCS)* produces a significant alteration of the species involved in the reaction whose key factor is represented by the shift from *Si* to $SiCl_2$ as the most important silicon precursor. While the former is the main chemical species responsible for

the homogeneous nucleation of silicon droplets in the gas phase, the latter is very stable and thus remains available to contribute to the film growth .
In this paper the experimental results of the growth rate and of the defects introduced during the epitaxial growth with these two new processes has been compared. The statistical results of Schottky diodes realized over epitaxial layers grown by HCl addition has been reported too.

Experimental

The epitaxial films were grown in a hot-wall reactor (built by LPE Epitaxial Technology) that can grow up to six 2 inch wafers and three 3 inch wafers at the same time. The chamber was studied to reduce the temperature ramp-up and ramp-down and the particulate formation. The substrates were 4H-SiC (0001), Si face, n-type (≅ 10^{18} cm^{-3}) off-axis (≅ 8° off towards the [1120] direction). These wafers were loaded into the reactor and the system was pumped down to a pressure of ≅10^{-5} Torr. The growth begins with a hydrogen etch sequence. At the deposition temperature *(1550-1650 °C)* the precursors *(SiH_4, HCl and C_2H_4)* are introduced into the hydrogen carrier gas and the growth starts at a fixed pressure of 100 Torr. The epitaxial layers were grown with different Si/H_2 and the obtained layers were analysed by Fourier Transform Infrared Reflectance (FTIR) for the thickness determination, mercury-probe C-V measurements for the doping concentration, AFM for surface roughness analysis, photoluminescence (PL), X-Ray Diffraction (XRD) rocking curve and chemical etch in molten KOH for defects quantification and distribution. Furthermore, PL was also used to detect the presence of 6H and 3C inclusions in the deposited layers.

On these wafers several Schottky diodes with different contact areas have been manufactured with a simple process using Ni_2Si as a Schottky barrier and a boron implanted edge termination. These diodes were characterized by I-V and C-V maps on the entire wafer to obtain the statistical information and spatial distribution of the defects. On selected diodes Deep Level Transient Spectroscopy (DLTS) was used to detect the levels introduced into the energy gap (not reported here).

Results and discussions

In Fig. 1 the growth rate *vs.* the *Si/H_2* ratio has been reported for a fixed Cl/Si ratio (Cl/Si=1). From these data can be observed that, while in the standard process (without chlorine addition) the growth rate is limited to 6-8 μm/h from the homogeneous silicon nucleation in the gas phase, in the new processes with chlorine addition very high growth rate (> 100 μm/h) can be reached without silicon precipitation. Furthermore, the growth rate increase vs. the Si/H_2 ratio does not seems to depend from the particular process used. In fact, for a fixed dilution ratio, the growth rate obtained with the process with the addition of HCl and that one with the substitution of SiH_4 with TCS gives the same growth rate within the experimental errors.

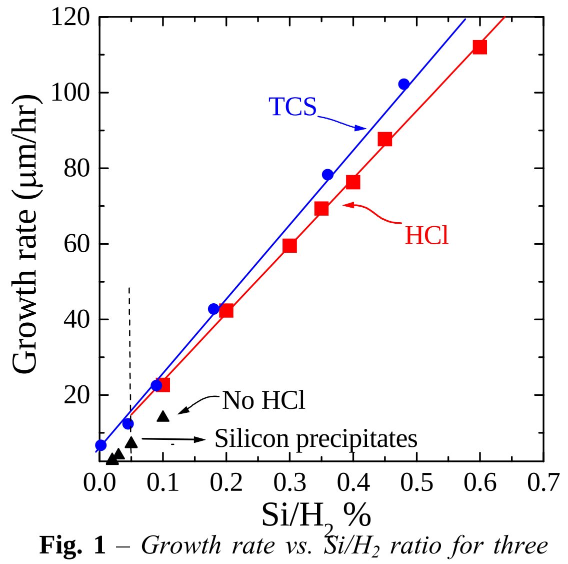

Fig. 1 – *Growth rate vs. Si/H_2 ratio for three different processes.*

These epitaxial layers growth with the new process has been characterized also by Atomic Force Microscopy (AFM) to measure the surface roughness. The average surface roughness, measured in several regions of the wafers, does not depend on the growth rate and is of about *0.3 nm* for all the samples. The same values are measured also for the standard process without *HCl*.
Comparing the dislocation density of the process with *HCl* addition or with TCS with respect to the standard process without hydrochloric acid by *KOH* etch at *500°C*, no large difference can be

observed between the different processes. In particular the screw dislocation densities are in the range between $4{\times}10^{2}$ cm^{-2} and $3{\times}10^{3}$ cm^{-2}. The edge dislocation densities are in the range between $3{\times}10^{4}$ cm^{-2} and $7{\times}10^{4}$ cm^{-2}. Finally the plane dislocations are between $2{\times}10^{3}$ cm^{-2} and $6{\times}10^{3}$ cm^{-2}.
With this process a high value of the minority carrier lifetime has been measured by a modified μ-PCD (built by Semilab) with an excitation light produced by a 350 nm wavelength laser. An average carrier lifetime of more than 1 μs, that is a very high value for SiC epitaxial layers, has been

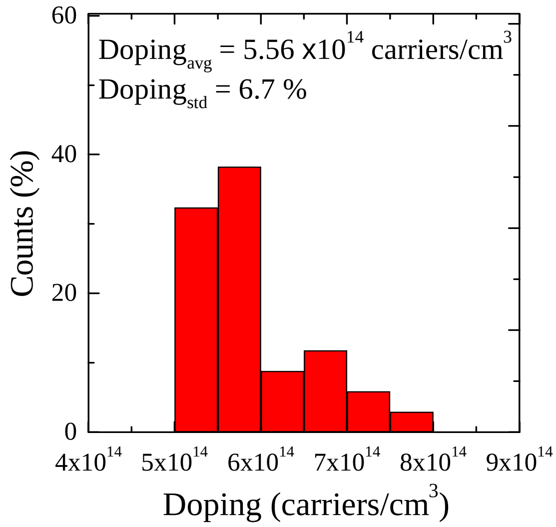

Fig. 2 – *Doping distribution over several wafers grown with the HCL process at high growth rate.*

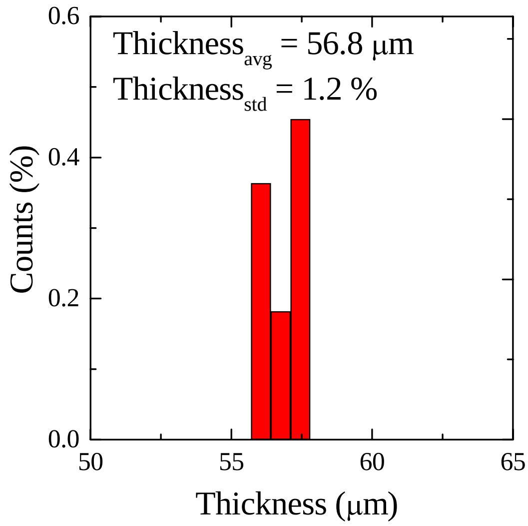

Fig. 3 – *Thickness distribution over several wafers grown with the HCL process at high growth rate.*

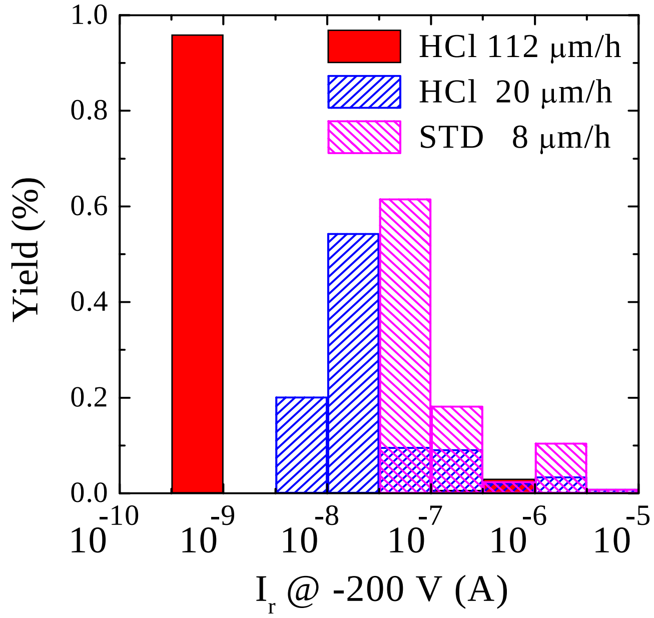

Fig. 4 *Leakage current distribution at -200 V for different epitaxial growth processes. The Schottky diodes area is fixed to 1 mm^2.*

measured. Then with this process good bipolar devices or X-Ray detectors can be obtained.
The high growth rate process gives also a low background doping levels (lower than $1{\times}10^{14}/cm^3$) and the possibility to obtain doped layers with low doping concentration with a good uniformity. In figure 2 a statistical distribution on several wafers grown with the same very high growth rate process (with TCS) has been reported. The average doping concentration for this process is $5.6{\times}10^{14}/cm^3$ and the standard deviation is the 6.7% of the average value.
Also the thickness uniformity of the high growth rate process (with TCS) is extremely good, as can be

observed in Fig. 3. In this figure the statistical distribution on several wafers grown on the same run are reported. The standard deviation of these measurements is the 1.2% of the average value.
Several Schottky diodes, with the process described in the previous section, were manufactured on different wafers with the epitaxial layers grown with the HCl addition or using the standard process without HCl. The leakage current distribution at 200 V on the entire wafer for the three different processes is compared in Fig. 4 for 1 mm^2 diodes. From this figure it can be observed that the leakage distribution of the HCl process at low growth rate (20 µm/h) is very close to the standard process in the current range between 10^{-8} and 10^{-4} A. The same distribution for the HCl process at high growth rate (112 µm/h) is even better and 95% of the diodes have a leakage current of the order of 10^{-9} A. This behaviour, as suggested from the results reported in our work on DLTS measurements[6], should be related to the concentration reduction of the level $EH_{6/7}$ that is responsible of the generation current. Furthermore the total yield of the wafer is higher than 85% and is comparable with the best results obtained with the standard epitaxial process on 1 mm^2 Schottky diodes realized with the same process.

Conclusions

The processes with HCl addition or with trichlorosilane *(TCS)* as silicon precursor source produce very high deposition rate *(> 100 µm/h)* with good surface morphology *(RMS ≈ 0.3 nm)*, high the minority carrier lifetime *(≈ 1 µs)* and good thickness and doping uniformity.
The Schottky diodes realized on the epitaxial layers grown with these processes show good electrical characteristics and high yield. Then these processes are extremely interesting for high voltage SiC devices with breakdown voltages of about *10 kV*.
In the next future these processes will be developed also for 3 and 4 inches wafers with 4 degree of off-axis.

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